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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/679,461	10/04/2000	Richard J. Ely	2494/103	5412

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EXAMINER
LI, ZHUO H

ART UNIT	PAPER NUMBER
2186	14

DATE MAILED: 08/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/679,461	ELY ET AL.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 6, 2003 (Paper no. 12) has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 32 is rejected under 35 U.S.C. 102(b) as being anticipated by Bauman et al (US PAT. 5,875,472 hereinafter Bauman).

Regarding claim 32, Bauman discloses an apparatus comprising a number of host applications (31,33,35,37 and 46, figure 2A), a memory device (54, figure 2A), wherein one ore more of the host applications (31,33,35 and 37, figure 2A) and memory device (54, figure 2A) have different interface requirements, i.e., each of the input circuit (104, figure 2) is associated with each host applications, respectively, each input circuit comprising segment selection logic (116, figure 3) which map the address into one of the segments in second level cache, two read

address registers (108 & 110, figure 3), and two write address register (112 & 114, figure 3), and all address signals are not provided to a respective input circuit at one time (col. 9 line 48 through col. 11 line 13), address/control interface (84 & 86, figure 2) are cross-bar interfaces that interconnect between the input circuits (104) and second level cache (50, figure 2) wherein each of lines 84 and 86 represent multiple address and control interfaces (col. 8 line 57 through col. 9 line 2 and col. 11 lines 14-42), in addition, each of the segment in second level cache further comprising memory interface line (264, figure 4) which provide address to memory device (col. 13 lines 5-16), and a memory interface device (28, figure 2A) interposed between the host applications and the memory device and operably coupled to receive memory access requests from the number of host application, interact with the memory device on behalf on the number of host applications for servicing the memory access requests in accordance with the interface requirements for the memory device, and provide result/status information to the host applications in accordance with the interface requirements for each of the number of host application (col. 7 line 54 through col. 9 line 47 and col. 17 line 39 through col. 19 line 46).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 3-12, 14, 17, 19-31, 33 and 35-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauman et al (US PAT. 5,875,472 hereinafter Bauman) in view of Hughes (US PAT. 5,784,582).

Regarding claim 1, Bauman discloses a memory interface device (28, figure 2A) for interfacing a number of host applications (31,33,35 and 37, figure 2A) to a memory device (54, figure 2A), the memory interface device comprising a host interface for interfacing with the number of host applications (col. 7 lines 62-64), a memory interface for interfacing with the memory device (col. 9 lines 43-47), wherein one ore more of the host applications (31,33,35 and 37, figure 2A) and memory device (54, figure 2A) have different interface requirements, i.e., each of the input circuit (104, figure 2) is associated with each host applications, respectively, each input circuit comprising segment selection logic (116, figure 3) which map the address into one of the segments in second level cache, two read address registers (108 & 110, figure 3), and two write address register (112 & 114, figure 3), and all address signals are not provided to a respective input circuit at one time (col. 9 line 48 through col. 11 line 13), address/control interface (84 & 86, figure 2) are cross-bar interfaces that interconnect between the input circuits (104) and second level cache (50, figure 2) wherein each of lines 84 and 86 represent multiple

address and control interfaces (col. 8 line 57 through col. 9 line 2 and col. 11 lines 14-42), in addition, each of the segment in second level cache further comprising memory interface line (264, figure 4) which provide address to memory device (col. 13 lines 5-16), a number of contexts (82, figure 2A) operably coupled to the host interface for receiving memory access requests from the number of host applications and providing result/status information to the number o host applications (col. 8 lines 43-53). Bauman differs from the claimed invention in not specifically teaches a control logic operably coupled to obtain memory access requests from the number of contexts, interact with the memory device over the memory interface for servicing the memory access requests on behalf of the number of host applications in accordance with the interface requirements for the memory device, and provide the result/status information to the number of host applications via the number of contexts in accordance with the interface requirements for each of the number of host applications. However, Hughes teaches a shared SDRAM arbiter/controller logic 72 in the shared SDRAM controller/arbiter 20, selects requests for the shared memory pipeline, and control and address signals are provided to the shared SDRAM (figure 2 and col. 5 lines 28-34). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Bauman in having a control logic operably coupled to obtain memory access requests from the number of contexts, interact with the memory device over the memory interface for servicing the memory access requests on behalf of the number of host applications in accordance with the interface requirements for the memory device, and provide the result/status information to the number of host applications via the number of contexts in accordance with the interface requirements for each of the number of

host applications, as per teaching of Hughes, because it provides a greater control over pipeline fullness and reduce the latency.

Regarding claim 3, Bauman discloses the memory device comprises a content-addressable memory (CAM), and wherein the memory interface conforms to a CAM interface (col. 8 lines 3-11 and col. 8 line 57 through col. 9 line 29).

Regarding claim 4, Bauman discloses the number of contexts comprises a number of context registers sets (104, figure 2).

Regarding claim 5, Bauman discloses each context register set corresponds to one and only one of the number of host applications (figure 2 and col. 8 lines 52-54).

Regarding claim 6, Hughes discloses the control logic comprises monitoring logic (104, 105, 106 and 107 in figure 3), schedule logic (108, figure 3), memory interface logic (111, figure 3), result/status logic (110, figure 3), wherein the monitoring logic is operably coupled to monitor the number of contexts for detecting memory access requests and providing the memory access requests to the scheduling logic (col. 5 lines 37-56), the scheduling logic is operably coupled to schedule memory access operations for the memory access requests (col. 5 lines 63-66), the memory interface logic is operably coupled to generate memory interface signals fro interfacing with the memory device over the memory interface (col. 5 lines 50-54), and the result/status logic is operably coupled to provide result/status information to the number of host applications (col. 5 lines 49-50).

Regarding claim 7, Bauman discloses each context comprises a context register set (104, figure 2), and wherein the monitoring logic is operably coupled to monitor a predetermined

register in each context register set to detect a memory access request (figure 3 and col. 10 line 58 through col. 11 line 13).

Regarding claim 8, Bauman discloses the predetermined register comprises an instruction register (col. 8 lines 43-51).

Regarding claim 9, Hughes discloses the memory interface supports pipelining of memory access operations, and wherein the scheduling logic is operably coupled to pipeline a plurality of memory access requests over the memory interface (col. 2 lines 21-31 and col. 5 lines 63-66).

Regarding claim 10, Hughes discloses the scheduling logic is operably coupled to determine that a plurality of memory access requests conflict and execute at least one of the conflicting memory access requests as an atomic operation (col. 2 lines 44-56).

Regarding claim 11, Bauman discloses the scheduling logic is operably couple to clear the pipeline in order to execute the conflicting memory access request as an atomic operation (col. 16 line 42 through col. 17 line 38).

Regarding claim 12, Hughes discloses the result/status logic is operably coupled to correlate result/status information with its corresponding memory access request (col. 5 lines 49-50).

Regarding claim 13, Bauman discloses the result/status logic is operatly coupled to store the result/status information for each memory access request in a corresponding context (col. 9 lines 39-41).

Regarding claim 14, Bauman discloses each context comprises a validity indicator, and wherein the result/status logic is operably coupled to set the validity indicator in each context

when the corresponding memory access is complete and the result/status information is available (col. 22 lines 31-35).

Regarding claim 15, Bauman discloses the memory interface device as programmed programmable logic device (28, figure 2A and 29, figure 2B).

Regarding claim 17, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 21, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 22, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 23, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claim 24, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Regarding claim 25, the limitations of the claim are rejected as the same reasons set forth in claim 9.

Regarding claim 26, the limitations of the claim are rejected as the same reasons set forth in claim 10.

Regarding claim 27, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claim 28, the limitations of the claim are rejected as the same reasons set forth in claim 12.

Regarding claim 29, the limitations of the claim are rejected as the same reasons set forth in claim 13.

Regarding claim 30, the limitations of the claim are rejected as the same reasons set forth in claim 14.

Regarding claim 31, Bauman discloses the program logic in a computer readable medium (col. 7 lines 54-58).

Regarding claim 33, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 35, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 36, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 37, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 38, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 39, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claim 40, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Regarding claim 41, the limitations of the claim are rejected as the same reasons set forth in claim 9.

Regarding claim 42, the limitations of the claim are rejected as the same reasons set forth in claim 10.

Regarding claim 43, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claim 44, the limitations of the claim are rejected as the same reasons set forth in claim 12.

Regarding claim 45, the limitations of the claim are rejected as the same reasons set forth in claim 13.

Regarding claim 46, the limitations of the claim are rejected as the same reasons set forth in claim 14.

Regarding claim 47, the limitations of the claim are rejected as the same reasons set forth in claim 15.

6. Claims 2, 16, 18, 34 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauman et al (US PAT. 5,875,472 hereinafter Bauman) and Hughes (US PAT. 5,784,582) as applied to claim 1 above, and further in view of Wentka et al. (US PAT. 5,968,114 hereinafter Wentka).

Regarding claim 2, the combination of Bauman and Hughes differs from the claimed invention in not specifically teaches the number of host applications comprises a number of packet processing contexts of a packet processor, and wherein the host interface conforms to a packet processor interface. However, Wentka teaches the processing elements (12, figure 1), comprises 32 separate processing elements 30 and 3 input/output processors (figure 5 lines 65-67), processor interface 50 conforms to a packet processor interface (figure 2, and col. 4 lines 1-6). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Bauman and Hughes in having the host applications comprises a number of packet processing contexts of a packet processor, and wherein the host interface conforms to a packet processor interface, as per teaching of Wentka because it provides to communicate data with the CPU's or processors utilizing the time division multiplexing.

Regarding claim 16, Wentka teaches the memory interface device as an application specific integrated circuit (col. 10 lines 23-28).

Regarding claim 18, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 34, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 48, the limitations of the claim are rejected as the same reasons set forth in claim 16.

Response to Arguments

7. Applicant's arguments filed August 6, 2003 (Paper no. 10) have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a host application interface may have a different bus width or interface cycle times than the memory device interface), are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In addition, Bauman discloses in the multiple processing system, having a plurality of instruction processors (31, 33, 35 and 37, figure 2A), memory device (54, figure 2A) and memory interface device (28, figure 2A), and each of the instruction processor having it's own associative input logic (104, figure 2A) wherein each of the input logic comprising segment selection logic, two read address registers and two write address registers which operatly based on the instructions/operands generated from the instruction processor and further generates different memory access requirement (i.e., all address signals are not provided to a respective input circuit at one time, col. 9 line 48 through col. 11 line 13), address/control interface (84 & 86, figure 2) are cross-bar interfaces that interconnect between the input circuits (104) and second level cache (50, figure 2) wherein each of lines 84 and 86 represent multiple address and control interfaces (col. 8 line 57 through col. 9 line 2 and col. 11 lines 14-42), in addition, each of the segment in second level cache further comprising memory interface line (264, figure 4) which provide address to memory device (col. 13 lines 5-16), and control logic (500, figure 7) further communicate with other elements in memory interface device, i.e., pointer control logic (240), conflict detect logic(234) and priority logic

(220), provides result/information to each respectively requested instruction processor with their different requirements (col. 17 line 39 through col. 19 line 46). Thus, the broad claimed limitation could be rejected by the combination of Bauman and Hughes.

Conclusion

8. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7239

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100